

Gen5 Hybrid Controller with SRIOV

Highly Configurable

Technology Independent

System Validated

Overview

Mobiveil's PCI Express® Hybrid (RC and EP) Controller is a highly flexible and configurable design targeted for implementations in datacenter, desktop, mobile, networking and AI/ML applications. The controller architecture is carefully tailored to optimize link utilization, latency, reliability, power consumption and silicon footprint.

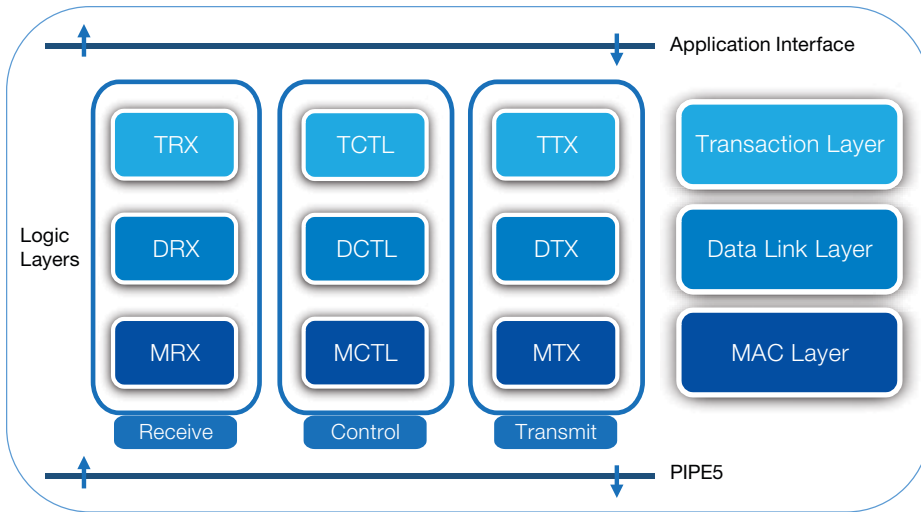
GPEX-HY is part of Mobiveil's PCI Express® (GPEX) family of IP solutions which includes Endpoint (GPEX-EP), Root Complex (GPEX-RC), Switch port Controller (GPEX-SW), Switch (GPEX-SWITCH), GPEX-AXI Bridge (GPEX-AXI) and GPEX-AHB Bridge (GPEX-AHB) designs.

The controller's simple, configurable and layered architecture is independent of application logic, PHY designs, implementation tools and most importantly, the target technology. Mobiveil solution allows the licensees to easily integrate into a wide range of applications. Mobiveil solution provides highly scalable bandwidth through configurable lanes, widths and frequencies.

GPEX-HY leverages Mobiveil's years of experience in PCI, PCI-X and HyperTransport technologies and the expertise in creating system validated IP solutions with RTL, synthesis, simulation, board and software elements to offer lowest risk in terms of compliance and inter operability.

Features

- Built to support PCIe® base specification 5.0 (32 Gbps per lane) and backward compatible with PCIe® versions 4.0, 3.1, 2.0 and 1.1
- Supports SR-IOV
- Supports to Address Translation Services
- Supports configurable number of PFs and VFs for SR-IOV
- Architected for high link utilization and low latency
- Efficient receive and transmit-retry buffering scheme
- Completely handles PCI Express® ordering rules
- Implements flow control logic in both directions
- Packet oriented user logic interface
- Supports PIPE 5 Compliant PHYs
- Flexible lane ordering and support for lane reversal
- Supports separate RefClk independent SSC architecture-SRIS
- L1 PM Sub-states (Low Power States) with CLKREQ#
- Supports Bifurcation



- Status : Gold
- Availability : Available now
- Language : Verilog
- Synthesis : DC, Genus, Quartus, Vivado
- Simulation : Cadence, Synopsys, Mentor
- Technology : 40nm ASIC or better, FPGA

Specification

Configurable Options

- Maximum Link Width (x1, x2, x4, x8, x16)
- Maximum TLP data payload size supported (128B to 4KB)
- Data Path Widths (32, 64, 128, 256, 512 bit)
- Transmit Retry/Receive Buffer size
- 8-bit/16-bit/32-bit/64 bit PIPE interface
- Number of Virtual Channels
- Upstream port / downstream port
- Inclusion of specific sublayers etc.
- ASPM L1 / Wake support, Auxiliary power support
- Hot plug support
- L1 PM Substate Support

Documentation

- Design Datasheet
- Verification Guide
- Synthesis Guide

Design Attributes

- Design Attributes
- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly demarked clock domains
- Software control for key features
- Multiple loop backs for debug

Product Package

- Verilog RTL Code
- UVM based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

About Mobiveil

Mobiveil is a fast-growing technology company that specializes in development of Silicon Intellectual Property (SIP), platforms and solutions for AI/ML, Flash Storage, Data Center, 5G Telecom, Automotive and Industrial IOT applications. The Mobiveil team leverages decades of experience to deliver high-quality, production-proven, high-speed serial interconnect SIP cores, and custom and standard form factor embedded platforms to leading companies worldwide. With a highly motivated engineering team, dedicated integration support, a flexible business model, strong industry presence through strategic alliances and key partnerships, Mobiveil solutions add value to users by matching their product goals on time and within budget. Mobiveil is headquartered in Silicon Valley with engineering development centers located in Milpitas, CA, Chennai, Bangalore and Hyderabad, in India, and sales offices and representatives located in the U.S., Europe, Israel, Japan, Taiwan and the People's Republic of China.

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Patents and Patents pending.

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