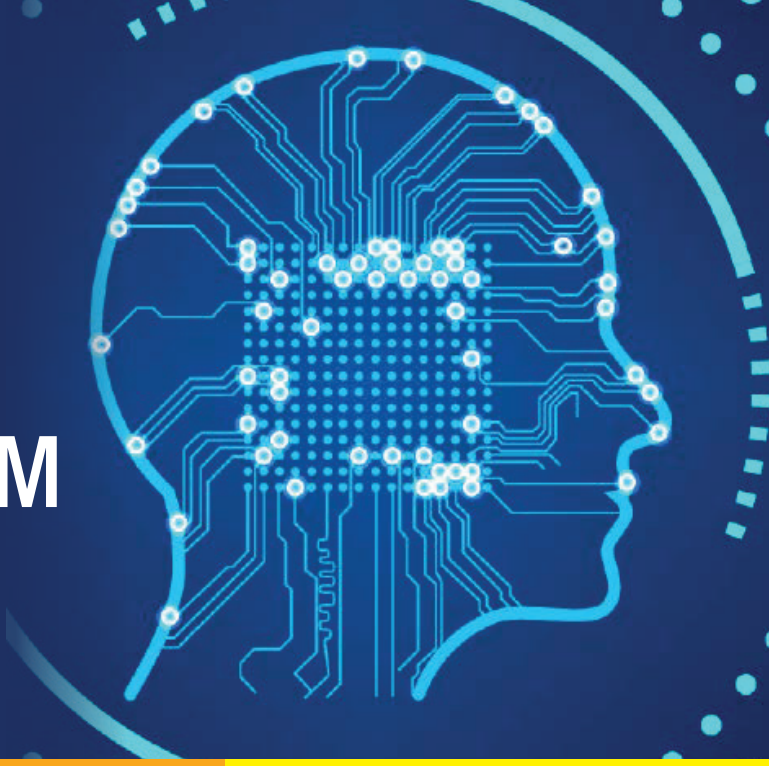
mobiveil
a GlobalLogic company



Octal SPI DDR PSRAM Controller

Highly Configurable | Technology Independent | System Validated

Overview

Most wearables devices typically monitor a finite set of parameters which does not demand a lot of computing power and memory size. Thus any wearable design requires low power, lower RAM density and simplified interface with optimal performances. These design requirements make PSRAM a natural choice for wearable applications. PSRAM has the advantages that there is no need of refresh control from external sources (unlike SDRAM) and active and standby currents are very low, therefore it has been adopted in many battery-operated mobile applications such as cellular phones and recently making its way into wearables and IoT applications.

Mobiveil's approach on this emerging scenario results in a PSRAM controller named "Octal SPI DDR PSRAM controller".

This controller supports AP Memory's Xccela open-standard Bus for digital interconnect and data communications, suitable for non-volatile and volatile memories such as PSRAM. This controller enables smooth integration AP Memory's of Xccela PSRAM memory chips into various new-gen devices made with mobile and wearable low power SoCs'. This memory controller implementation is designed to give the user full flexibility for driving the memory control signals and timing adjustment for data sampling.

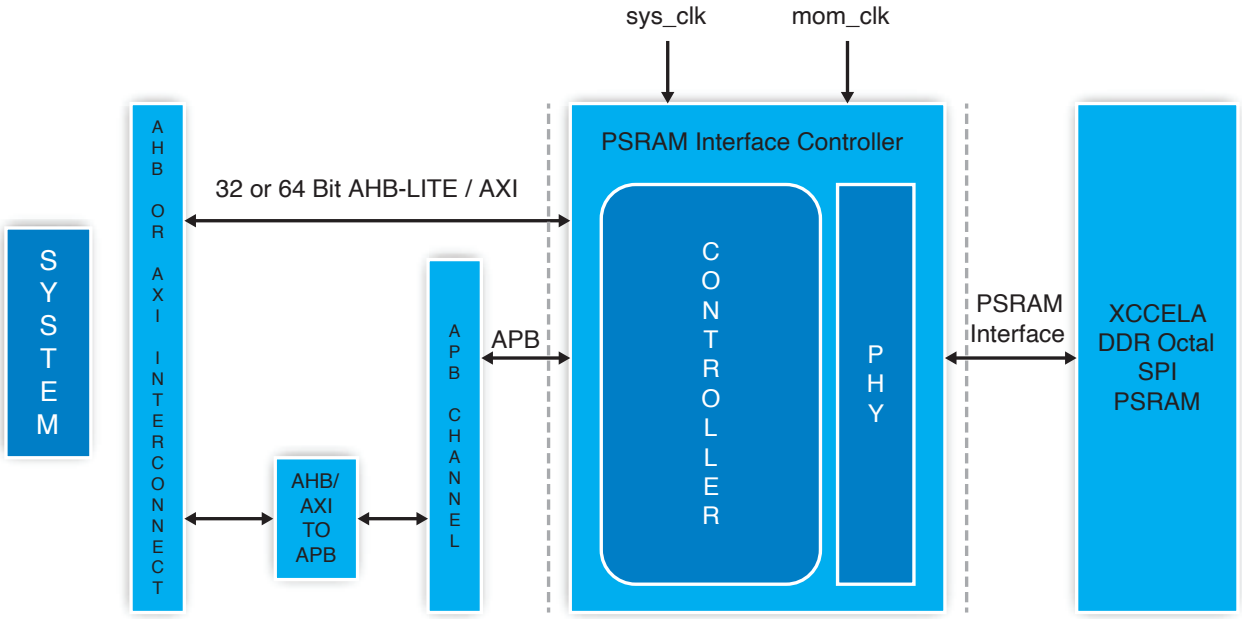
Features

Device Supported:

- Compatible with following Xccela PSRAM devices from APMemory
  - 8 bit data bus – DQ[7:0] support for APSxx08L-0B device, where xx stands for memory density
  - 16 bit data bus – DQ[15:0] support for APSxxyyN device, where yy stands for I/O config
  - Possible values: xx=64, 128, 256 and yy=08, 16
- Compatible with APS3208K device from APMemory

Other Features:

- Memory mapped access to the connected PSRAM Device
- Octal SPI Interface with **DDR** mode access support
- Wrap transfer support
- Continuous mode Burst transfer support for efficient memory access
- Hybrid wrap burst transfer support
- AXI4 system interface for memory access with outstanding address support. Alternatively, AHB Lite system interface for memory access
- APB port for control registers accesses
- Read-Prefetch feature for efficient read data throughput in AHB-Lite flavour
- Half sleep and deep power down control through simple CSR access
- Behavioral reference PHY model for easier technology specific integration and implementation



- Status : Gold
- Availability : Q1, 2018
- Contact : ip@mobiveil.com
- Language : Verilog
- Synthesis : Synopsys DC, Synplicity
- Simulation : Cadence, Synopsys, Mentor

Specification

Design Attributes

- Highly modular and programmable design
- Fully synchronous design
- Software control for key features

Product Package

- RTL Code
- System Verilog/UVM based Testbench
- Test cases
- Protocol checkers and bus watchers

Documentation

- Design Guide
- Verification Guide
- Synthesis Guide

Licensing Options

- Single Design or Multi-project license (HDL Source Code).

About Mobiveil

Mobiveil is a fast-growing technology company that specializes in development of Silicon Intellectual Property (SIP), platforms and solutions for AI/ML, Flash Storage, Data Center, 5G Telecom, Automotive and Industrial IoT applications. The Mobiveil team leverages decades of experience to deliver high-quality, production-proven, high-speed serial interconnect SIP cores, and custom and standard form factor embedded platforms to leading companies worldwide. With a highly motivated engineering team, dedicated integration support, a flexible business model, strong industry presence through strategic alliances and key partnerships, Mobiveil solutions add value to users by matching their product goals on time and within budget. Mobiveil is headquartered in Silicon Valley with engineering development centers located in Milpitas, CA, Chennai, Bangalore and Hyderabad, in India, and sales offices and representatives located in the U.S., Europe, Israel, Japan, Taiwan and the People's Republic of China.

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